This Listing of Claims will replace all prior versions or listings of claims in this application.

LISTING OF CLAIMS

1. (Currently Amended) A communication device, comprising:

~~a central processing unit electrically connected to A address lines and M data lines of a processor bus, wherein the A address lines convey A bits of an address in parallel and the M data lines convey M bits of data in parallel;~~

~~a packet bus having;~~

~~control lines for conveying control signals; and~~

~~N bidirectional data lines for conveying a command packet and for conveying a data packet including the M bits of data, wherein each of A and M is greater than N, and wherein A, M and N are integers; and~~

a signal modulator/demodulator (modem) having a digital signal processor for effecting radio communications;

an application processor (AP) having a central processing unit and a bus master controller~~, electrically connected to the A address lines and M data lines of the processor bus and to the control lines and the N bidirectional data lines of the packet bus,~~ for controlling via ~~the packet~~ a first common bus a plurality of extermal peripherals ~~electrically connected to the control lines and the N bidirectional data lines of the packet bus.~~; and

a shared memory connected to the AP via the first common bus and connected to the

modem via a second common bus,

wherein the bus master controller controls the plurality of external peripherals by using a packet generator issuing a packetized command commonly receivable by the plurality of external peripherals over the first common bus, and wherein the packetized command includes a module device select signal for selecting one of the plurality of external peripherals.

2. (Canceled)

3. (Currently Amended) The device of claim ~~2, further comprising:~~

~~a signal modulator/demodulator, for effecting radio communications, having an interface operatively connected to a memory shared by the modem and by the central processing unit, wherein the memory is operatively connected to and on the packet bus and not directly connected to the processor bus~~ 1, wherein the shared memory is an SDRAM.

4. (Currently Amended) The device of claim 1, wherein the plurality of external peripherals ~~operatively connected to and on the packet bus includes a memory shared by the central processing unit and by a signal modulator/demodulator for effecting radio communications, and~~ include at least one of an image capture module, a display, and a flash memory.

5. (Canceled)

6. (Currently Amended) The device of claim ~~5~~1, wherein the selected one of the plurality of external peripherals returns a signal to the bus master controller to acknowledge receipt of the packetized command ~~packet~~.

7. (Currently Amended) The device of claim ~~5~~1, wherein the packetized command packet includes:

a read/write command directed to ~~a~~ shared memory shared by the modem and the ~~central processing unit;~~

~~a field that specifies the length of a data packet; and~~

~~a field that indicates the start address of the commanded data read/write~~AP.

8. (Currently Amended) The device of claim 7, wherein data read from the shared memory is sent to the ~~central processing unit~~ AP with a strobe signal, and wherein the strobe signal is used for strobing the data read into a register in the bus master controller.

9. (Currently Amended) The device of claim 3, wherein the ~~control lines of the packet bus include:~~

~~a first signal line for conveying a first control signal that indicates that the N bidirectional data lines currently carry a command packet or a data packet; and~~

~~a second signal line for conveying a second control signal that indicates the current transfer direction over the N bidirectional data lines; and~~

~~a forward clock line for conveying a control signal for synchronizing write data packets.~~ SDRAM includes a plurality of data banks and an interface for interfacing the bus

master controller via the first common bus.

10. (Currently Amended) The device of claim 3, wherein the shared memory includes a first protection circuit for receiving address data from the ~~central processing unit~~ AP and a second protection circuit for receiving address data from the ~~signal modulator/demodulator and~~ modem, each for generating a protect signal upon simultaneously receiving the same address from the ~~signal modulator/demodulator~~ modem and the ~~central processing unit~~ AP, wherein the protect signal is generated to halt memory access by one of the ~~signal modulator/demodulator~~ modem and the ~~central processing unit~~ AP in order to prevent simultaneous access of the same memory cells ~~by both of the signal modulator/demodulator and the central processing unit~~.

11. (Currently Amended) A communication device, comprising:

~~a central processing unit operatively connected to A address lines and M data lines of a processor bus, wherein the A address lines convey A bits of an address in parallel and the M data lines convey M bits of data in parallel;~~

a signal modulator/demodulator~~,~~ (modem) having a digital signal processor for effecting radio communications;

~~a memory shared by the modulator/demodulator and by the central processing unit;~~

~~a first packet bus having:~~

~~control lines for conveying control signals; and~~

~~N bidirectional data lines for conveying a command packet and for conveying~~

~~data packets including the M bits of data, wherein each of A and M is greater than N, and wherein A, M and N are integers;~~

~~a second packet bus having control lines and N data lines for conveying a command packet and a data packet including the M bits of data; and~~

~~a first~~ an application processor (AP) having a central processing unit and a bus master controller~~, electrically connected to A address lines and M data lines of the processor bus and to the control lines and N bidirectional data lines of a first packet bus~~ for controlling via ~~the~~ a first ~~packet~~ common bus ~~at least one peripheral on the first packet bus~~connected to a plurality of external peripherals; and

~~a second master controller, electrically connected to the control lines and N bidirectional data lines of the second packet bus, for controlling via the second packet bus the~~

a shared memory ~~shared by~~ connected to the AP via the first common bus and connected to the ~~modulator/demodulator and by the central processing unit~~modem via a second common bus,

wherein the bus master controller further controls a flash memory via the first common bus.

12. (Canceled)

13. (Currently Amended) The device of claim 11, wherein ~~the~~ at least one peripheral ~~on the first packet bus~~ of the plurality of external peripherals is an image capture module.

14. (Currently Amended) The device of claim 11, wherein the ~~first~~ bus master controller ~~is configured to control a~~ controls the plurality of external peripherals operatively connected to the first ~~packet~~ common bus by issuing a packetized command ~~packet~~ commonly receivable by the plurality of external peripherals over the ~~N bidirectional data lines of the~~ first ~~packet~~ common bus, and wherein the packetized command ~~packet~~ includes a module device select signal for selecting one of the plurality of external peripherals.

15. (Currently Amended) The device of claim 14, wherein the selected one of the plurality of peripherals returns a signal over the ~~control lines of the~~ first ~~packet~~ common bus to the ~~first~~ bus master controller in the AP to acknowledge receipt of the packetized command ~~packet~~.

16. (Currently Amended) The device of claim 14, wherein ~~a~~ the packetized command ~~packet directed to the memory shared by the modem and the central processing unit~~ includes:

~~a field specifying a Read Transfer or a Write Transfer;~~

~~a field that specifies the length of a data packet; and~~

~~a field that indicates the start address of the requested transfer~~a read/write command to the shared memory connected to the AP and the modem.

17. (Currently Amended) The device of claim 16, wherein data read from the shared memory is transmitted via the first common bus to the ~~first~~ bus master controller in the AP with a strobe signal, and wherein the strobe signal is for strobing the data read into a

register in the ~~first~~ bus master controller.

18. (Currently Amended) The device of claim 11, wherein ~~M is an integer multiple of N~~the shared memory is an SDRAM.

19. (Currently Amended) The device of claim 18, wherein ~~N is four~~ the SDRAM includes a plurality of data banks and an interface for interfacing .

20. (Currently Amended) The device of claim 18, wherein ~~the control lines of the first packet bus include:~~

~~a signal line that indicates whether the N bidirectional data lines currently carry a command packet or a data packet;~~

~~a signal line that indicates the current transfer direction over the N bidirectional data lines.~~

the SDRAM includes a first protection circuit for receiving address data from the AP and a second protection circuit for receiving address data from the modem and for generating a protect signal upon simultaneously receiving the same address from the modem and the AP.

21. (Currently Amended) An application processor (AP), for use in a communication device, comprising:

a central processing unit~~, operatively connected to a processor bus including A address lines and M data lines,~~ for processing data received from a plurality of external peripherals~~, wherein the A address lines convey A bits of an address in parallel and the M data lines~~

~~convey M bits of data in parallel~~; and

a ~~first~~ bus master controller ~~electrically connected to the M data lines of the processor bus and to the N bidirectional data lines of a first packet bus,~~ for controlling via ~~the~~ a first ~~packet~~ common bus ~~a~~ the plurality of external peripherals~~;~~,

~~wherein the first packet bus includes:~~

~~control lines for conveying control signals; and~~

~~N bidirectional data lines for conveying a command packet and for conveying a data packet including the M bits of data, wherein each of A and M is greater than N, and wherein A, M and N are integers~~and for interfacing with a shared memory that is connected to a signal modulator/demodulator (modem) via a second common bus.

22. (Canceled)

23. (Currently Amended) The device of claim ~~22~~21, wherein ~~the modulator/demodulator (modem) includes a second master controller, and the shared memory and the second master controller are operatively connected to each other via a second packet bus having:~~

~~control lines for conveying control signals; and~~

~~N bidirectional data lines for conveying a command packet and for conveying data packets.~~

the shared memory is an SDRAM.

24. (Currently Amended) The device of claim 21, wherein the plurality of external

peripherals additionally includes at least one of an image capture module, a display, and a flash memory.

25. (Currently Amended) The device of claim 21, wherein the ~~first~~ bus master controller controls the plurality of peripherals by issuing a packetized command ~~packet~~ commonly receivable by the plurality of external peripherals over the ~~N bidirectional data lines of the packet~~ first common bus, and wherein the packetized command includes a module device select signal used for selecting one of the plurality of external peripherals.

26. (Currently Amended) The device of claim 25, wherein the selected one of the plurality of external peripherals returns a signal to the bus master controller over the first common bus to acknowledge receipt of the packetized command ~~packet~~.

27. (Currently Amended) The device of claim 25, wherein the packetized command ~~packet~~ includes:

~~a field specifying a Read Transfer or a Write Transfer;~~

~~a field that specifies the length of a data packet; and~~

~~a field that indicates the start address of the requested transfer~~a read/write command to the shared memory.

28. (Currently Amended) The device of claim 27, wherein the ~~command packet includes a module device select signal used for selecting one of the peripherals~~ data read from the shared memory is sent over the first common bus to the AP with a strobe signal, and

wherein the strobe signal is used for strobing the read data into a register of the bus master controller.

29. (Currently Amended) The device of claim 23, wherein the ~~shared memory is an~~ SDRAM ~~that~~ includes a plurality of data banks and ~~a first~~ an interface for interfacing the ~~first~~ bus master controller ~~via the N bidirectional data lines of the first packet bus, and a second interface for interfacing the second master controller in the modulator/demodulator via the N bidirectional data lines of the second packet bus~~.

30. (Currently Amended) The device of claim 23, wherein ~~N is four~~ the SDRAM includes a first protection circuit for receiving address data from the AP over the first common bus and a second protection circuit for receiving address data from the modem over the second common bus and for generating a protect signal upon simultaneous receipt of the same address from the AP and the modem.

31. (Currently Amended) ~~A~~ An application processor (AP) for use in a communication device comprising:

a central processing unit~~, operatively connected to a processor bus including A address lines and M data lines,~~ for processing data received from a plurality of external peripherals~~, wherein the A address lines convey A bits of an address in parallel and the M data lines convey M bits of data in parallel~~ over a first common bus; and

a ~~first~~ bus master controller ~~operatively connected to the processor bus and to a first packet bus having N data lines~~ for controlling via the first ~~packet~~ common bus the plurality

of external peripherals~~;~~

~~a second master controller operatively connected to the processor bus and to a second packet bus having N data lines, for controlling the signal modulator/demodulator (modem) via the second packet bus;~~

~~wherein each of the first packet bus and second packet bus includes:~~

~~control lines for conveying control signals; and~~

~~N bidirectional data lines for conveying a command packet and for conveying data packets including the M bits of data, wherein each of A and M is greater than N, and wherein A, M and N are integers.~~ and for interfacing with a shared memory that is connected to a signal modulator/demodulator (modem) via a second common bus.

32. (Canceled)

33. (Currently Amended) The device of claim ~~32~~ 31, wherein the shared memory is an SDRAM ~~that includes a plurality of data banks and a first interface for interfacing the second master controller via the N bidirectional data lines of the second packet bus, and a second interface for interfacing a third master controller in the modulator/demodulator via the N bidirectional data lines of a third packet bus~~.

34. (Currently Amended) The device of claim 31, wherein the plurality of external peripherals ~~on the first packet bus~~ include at least one of an image capture module, a display, and a flash memory.

35. (Currently Amended) The device of claim 31, wherein the ~~first~~ bus master controller controls the plurality of external peripherals ~~on the first packet bus~~ by issuing a packetized command ~~packet~~ commonly receivable by the plurality of external peripherals over the first ~~packet~~ common bus, and wherein the packetized command ~~packet~~ includes a module device select signal for selecting one of the plurality of external peripherals.

36. (Currently Amended) The device of claim 35, wherein the selected one of the peripherals returns a signal over the first common bus to the master controller to acknowledge receipt of the packetized command ~~packet~~.

37. (Currently Amended) The device of claim 35, wherein the packetized command ~~packet~~ includes a read/write command directed to ~~a~~ the shared memory shared by the modem and the ~~central processing unit~~AP.

38. (Currently Amended) The device of claim 37, wherein the ~~command packet further includes:~~

~~a field that specifies the length of a data packet; and~~

~~a field that indicates the start address of the requested transfer.~~ data read from the shared memory is sent to the AP over the first common bus with a strobe signal, and wherein the strobe signal is used for strobing the data read into a registor in the bus master controller.

39. (Currently Amended) The device of claim 33, wherein the ~~control lines of the first packet bus include:~~

~~a signal line that indicates whether the N bidirectional data lines currently carry a command packet or a data packet;~~

~~a signal line that indicates the current transfer direction over the N bidirectional data lines~~ SDRAM includes a plurality of data banks and an interface for interfacing with the bus master controller over the first common bus.

40. (Currently Amended) A method of controlling a communication device having a signal modulator/demodulator (modem) for effecting radio communications ~~and~~, an application processor (AP) having a central processing unit, and a bus master controller, and a shared memory, the method comprising:

controlling ~~the master controller~~ via a ~~processor~~ first common bus ~~having A address lines and M data lines of a processor bus, wherein the A address lines convey A bits of an address in parallel and the M data lines convey M bits of data in parallel;~~

~~using the master controller to control~~ a plurality of external peripherals ~~including the signal modulator/demodulator by issuing command packets via a packet bus operatively connected to the master controller and to each of the plurality of peripherals, wherein the packet bus is characterized by having:~~

~~control lines for conveying control signals; and~~

~~N bidirectional data lines for conveying the command packet and for conveying a data packet including the M bits of data, wherein each of A and M is greater than N, and wherein A, M and N are integers.~~ using the bus master controller; and

interfacing with the modem via the shared memory and a second common bus.

41. (Canceled)

42. (Currently Amended) The method of claim 40, wherein the shared memory is an SDRAM ~~that includes a plurality of data banks and a first interface for interfacing the master controller via the N bidirectional data lines of the packet bus, and a second interface for interfacing a second master controller in the modulator/demodulator via the N bidirectional data lines of a second packet bus~~.

43. (Currently Amended) The method of claim 40, wherein the ~~plurality of peripherals~~ step of controlling includes controlling at least one of an image capture module, a display, and a flash memory included in the plurality of external peripherals.

44. (Currently Amended) The method of claim 40, wherein the step of controlling the plurality of external peripherals includes issuing a packetized command ~~packet~~ commonly receivable by the plurality of external peripherals over the ~~packet~~ first common bus, and wherein the packetized command ~~packet~~ includes a module device select signal for selecting one of the plurality of external peripherals.

45. (Currently Amended) The method of claim 44, wherein the selected one of the plurality of external peripherals returns a signal to the bus master controller over the first common bus to acknowledge receipt of the packetized command ~~packet~~.

46. (Currently Amended) The method of claim 40, wherein the packetized command ~~packet~~ includes a read/write command directed to ~~a~~ the shared memory ~~shared by~~

~~the modem and the central processing unit~~.

47. (Currently Amended) The method of claim 46, wherein data read from the shared memory is transmitted over the first common bus to the ~~central processing unit~~ AP with a strobe signal, and wherein the strobe signal is for strobing the data read into a register in the bus master controller.

48. (Currently Amended) The method of claim 41, further including receiving address data from the AP over the first common bus and the modem over the second common bus at the shared memory and generating a protect signal upon simultaneously receiving the same address ~~in a command packet from the modem's master controller and in a command packet from the central processing unit's master controller, wherein the protect signal is generated to halt memory access by one of the signal modulator/demodulator and the central processing unit in order to prevent simultaneous access of the same memory cells by both of the signal modulator/demodulator and the central processing unit~~from the modem and the AP.

49. (Canceled)

50. (Canceled)